IN THE SPECIFICATION:

Please replace paragraph 0007 of the specification with the following amended paragraph.

One embodiment of the present invention provides a Phase-Locked Loop with multiphase clocks. The Phase-Locked Loop includes a main loop, a calibration loop, and Control Logic. The main loop includes, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider. The calibration loop is coupled to the Phase Frequency Detector, and comprises a Calibration Charge Pump, a ~~Multiplexer~~ Demultiplexer and Y Calibration Loop Filters, with Y being an integer. The Control Logic controls the Phase-Switching Fractional Divider and the ~~Multiplexer~~ Demultiplexer. A Reference Frequency Signal is coupled to the Phase Frequency Detector and a Calibration Signal is coupled to the calibration loop. The main loop further comprises a Phase-adjusting Block coupled to a ~~Demultiplexer~~ Multiplexer. The Phase-adjusting Block is arranged so as to receive at least one correction signal from the calibration loop. Preferably, the Control Logic also controls the Demultiplexer.

Please replace paragraphs 0018 to 0019 of the specification with the following amended paragraphs.

Fig. 1 shows the prior art solution. As shown, a first (Main) loop comprises, coupled in cascade, a Phase Frequency Detector (PFD) 1, a Main Charge Pump 2, a Main Loop Filter 3, a Multi-Phase Voltage Controlled Oscillator (VCO) 4 and a Phase-switching Fractional Divider 5. A second (Calibration) loop comprises the series connection of a Calibration Charge Pump 6, a ~~Multiplexer~~ Demultiplexer 7 and Y Calibration Loop Filters 8, with Y being an integer, coupled between the Phase Frequency Detector (PFD) 1 and the Multi-Phase Voltage Controlled Oscillator (VCO) 4. The ~~Multiplexer~~ Demultiplexer 7 is controlled by Control Logic 9 coupled to the Phase-Switching Fractional Divider 5. A Reference Frequency Signal 10 is applied to the Phase Frequency Detector 1. The Calibration signal 11 is applied to a control input of the Control Logic 9.

Fig. 2 shows the block scheme of one embodiment of the present invention. The Main Loop 1 5 remains the same. The second (Calibration) loop still comprises the series connection

of a Calibration Charge Pump 6, a ~~Multiplexer~~ Demultiplexer 7 and Y Calibration Loop Filters 8, with Y being an integer. The input still comes from the Phase Frequency Detector (PFD) 1, but the output is not connected to the Multi-Phase Voltage Controlled Oscillator (VCO), but is instead connected to a phase-adjusting block 12 that is positioned after the Phase-Switching Fractional Divider 5, i.e., at lower frequency. As in the prior art (Fig.1), the Control Logic 9 selects the correct loop filter [1:Y] of the phase to be calibrated, based on the state that the Phase-Switching Fractional Divider 5 is in. This is done with the ~~multiplexer~~ demultiplexer following the calibration charge pump 6. Additionally, the same Control Logic 9 also selects in the phase-adjusting block 12 the corresponding low-frequency delay cell T[1:Y] that is associated with this phase. This is done with the ~~de-multiplexer~~ multiplexer 13 shown in the block diagram.

Please delete the paragraph beginning at page 14, line 2 of the specification (abstract).

Please replace the paragraph beginning at page 14, line 4 of the specification (abstract) with the following amended paragraph.

A Phase-Locked Loop with multiphase clocks is provided. The Phase-Locked Loop includes a main loop, a calibration loop, and Control Logic. The main loop includes, coupled in series, a Phase Frequency Detector, a Main Charge Pump, a Main Loop Filter, a Multi-Phase Voltage Controlled Oscillator and a Phase-switching Fractional Divider. The calibration loop is coupled to the Phase Frequency Detector, and comprises a Calibration Charge Pump, a ~~Multiplexer~~ Demultiplexer and Y Calibration Loop Filters, with Y being an integer. The Control Logic controls the Phase-Switching Fractional Divider and the ~~Multiplexer~~ Demultiplexer. A Reference Frequency Signal is coupled to the Phase Frequency Detector and a Calibration Signal is coupled to the calibration loop. The main loop further comprises a Phase-adjusting Block coupled to a ~~Demultiplexer~~ Multiplexer. The Phase-adjusting Block is arranged so as to receive at least one correction signal from the calibration loop.